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[PDF] [XAPP246 "PowerPC 60X Bus Interface to a Virtex-E Device" v1.0 \(...](#)

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... Pipeline The address pipeline permits overlapping address **bus transactions** on the ... environment, the designer is extremely productive at generating **test cases**. ...
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... transfer of data rather than adding additional latency in the PCI **bus transactions**. ... in the SPACE 2 platform and measured its performance in **test cases** and when ...
www.cis.unisa.edu.au/~cisdak/ResearchPapers/ACACHigh1999.ps - [Similar pages](#)

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... language code. Simulation environments for ASICs may have **test cases** written in terms of **bus transactions**. The translation process ...
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... years running at operational speed to hit all the interesting **test cases**. ... to do exhaustive testing of the effects of various **bus transactions** interacting with ...
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... the number of clock cycles used to perform various **bus transactions** and can ... part (test_sw) of this example consists of several **test-cases** to interactively ...
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... **Transactions** 33Mhz @ 32 bits Utopia I @ 32 bits @ 8 bits Device Under Test (DUT) 125Mhz Micron Models 25Mhz ATM Packet Generator System Testbench **test cases** ...
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... The testbench provides menu driven **test cases** implementing the Libraries. ... The **bus**

transactions created by the DMA/XOR block are handled by the controllers. ...

www.intel.com/design/iio/papers/25367501.pdf - [Similar pages](#)

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... such as read() or write() and translates them into **bus transactions** that model ... must be given to guard against duplicate, irrelevant, and illegal **test cases**. ...

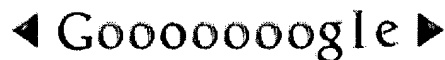
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[PDF] Testbench Design, A Systematic Approach.

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... Its role is to make sure that the **bus transactions** issued by upper V_Layers will reach the DUT, regardless of how the DUT is represented. ...

www.synopsys.com/sps/pdf/paper2.pdf - Nov 29, 2003 - [Similar pages](#)



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[PDF] [Coverage-Oriented Verification of Banias](#)

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... random testing, without embellishing corner cases or careful crafting delicate

test

cases. ... we required the coverage of back-to-back **bus transactions** that were ...

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... protocols are used to specify the exact manner in which **bus transactions** occur. ... profiles
for the MAC processor for a large number of **test cases**, consisting of ...

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[PDF] [Functional Verification of the HP PA 8000 Processor](#)

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... 1 Each job ran several thousand **test cases** that were generated using a ... emulate the
functionality required to initiate and respond to **bus transactions**, but the ...

cpus.hp.com/technical_references/functional_verification.pdf - [Similar pages](#)

[PDF] [1394.1 Standards Meeting Minutes](#)

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... you must wait for a (broadcast) notification before you resume off-**bus transactions**. ... 1.11.4

Presenter: David V. James, Sony Σ Slides of **test cases** needed to ...

grouper.ieee.org/groups/1394/1/Minutes/jul99.pdf - [Similar pages](#)

[PDF] [Debug Methodology for the McKinley Processor](#)

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... Small **test cases** of 100's of instructions are run on the processor ... that it would
fail to properly operate during initial **bus transactions** immediately after ...

www.intel.com/design/itanium2/download/debug_paper.pdf - [Similar pages](#)

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<html> <head> </head><body><pre><html> <head> </ ...

... since it is either returning data or forwarding XMI2 **bus transactions** for potential ... in
catching two design flaws that the focused **test cases** had missed. ...

research.compaq.com/wrl/DECarchives/DTJ/DTJ704/DTJ704SC.TXT - 45k - [Cached](#) - [Similar pages](#)

[PDF] [TeX output 1995.03.21:1529](#)

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... A bus demon might generate random (but legitimate) **bus transactions** while the connected
CPU ... they bias the random selection of system- level **test cases** in the ...

www-inst.eecs.berkeley.edu/~cs152/handouts/clark-test.pdf - [Similar pages](#)

[Verification Guild Archive, Vol 2, no 9](#)

... the automatic generation of assembly language instructions or streaming together

bus transactions. ... and you have the ability to have **test cases** steer themselves ...
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[PS] [Contrasting Hardware and Software Solutions to False Sharing on](#)

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... **Bus transactions** By keeping track of the number of **bus transactions** we hoped ... very deterministic pattern of sharing, which make them ideal **test cases** for Thor's ...

www.bergs.com/stefan/548/report.ps - [Similar pages](#)

[Functional verification of the POWER4 microprocessor and POWER4 ...](#)

... created several years ago to help us gauge the effectiveness of our **test cases**. ... It can analyze and report on a series of **bus transactions**, looking for specific ...

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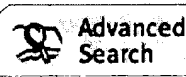
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 Rob Calvin. **Computer Technology Review**. Los Angeles: Nov 2002. Vol. 22, Iss. 11; p. 14 (3 pages)
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- ☐ 13. **TRADE NEWS: Agilent Technologies' New High-Speed Logic Analyzer Modules and Probes Provide Industry-Leading Insight for Emerging Technologies**
 Business Editors/High-Tech Writers Intel Developer Forum 2002. **Business Wire**. New York: Sep 9, 2002. p. 1
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- ☐ 14. **Co-verification speeds SOC design**
 Jason Andrews. **EDN**. Boston: Sep 5, 2002. Vol. 47, Iss. 19; p. 95 (4 pages)
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 Dominic Jones. **Asset Finance International**. London: Jun 2002. p. 12
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19. **Get on the bus**


- ☐ *Richard Ball. Electronic News.* New York: May 27, 2002. Vol. 48, Iss. 22; p. 18 (2 pages)


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PR Newswire. New York: May 6, 2002. p. 1

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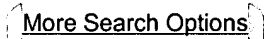


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Rajeev Jog , Philip L. Vitale , James R. Callister

ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems April 1990

Volume 18 Issue 1

This paper describes an approximate Mean Value Analysis (MVA) model developed to project the performance of a small-scale shared-memory commercial symmetric multiprocessor system. The system, based on Hewlett Packard Precision Architecture processors, supports multiple active user processes and multiple execution threads within the operating system. Using detailed timing for hardware delays, a customized approximate closed queueing model is developed for the multiprocessor system ...

- 2** Balancing performance and flexibility with hardware support for network architectures 77%



Ilija Hadžić , Jonathan M. Smith

ACM Transactions on Computer Systems (TOCS) November 2003

Volume 21 Issue 4

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

- 3** Simulation coverage and generation for verification: Coverage-oriented verification of banias 77%



Alon Gluska

Proceedings of the 40th conference on Design automation June 2003

The growing complexity of state-of-art microprocessors dictates the use of cost-effective verification methods. Functional coverage was widely applied in the verification of Banias, Intel's new IA-32 microprocessor designed solely for the mobile computing market. In this paper, we describe the practical coverage approach as was carried out in the verification of Banias. According to this Coverage-Oriented verification approach, focus shifts gradually from basic logic cleanup using random testing ...

4 MEDEA workshop: Fine-grain design space exploration for a cartographic 77%



SoC multiprocessor

Alessio Bechini , Pierfrancesco Foglia , Cosimo Antonio Prete

ACM SIGARCH Computer Architecture News March 2003

Volume 31 Issue 1

Traditionally, in the field of embedded systems low power consumption and low cost have been always regarded as stringent specification constraints. In recent years, high computational power has become a fundamental requirement as well. This has been mainly determined by the introduction of new features, typical of general-purpose systems, e.g. GUI-based interfaces. In this setting, low cost, low power consumption, significant computational power and short time-to-market are conflicting needs th ...

5 An architecture for mostly functional languages 77%



Tom Knight

Proceedings of the 1986 ACM conference on LISP and functional programming

August 1986

6 Synchronization with multiprocessor caches 77%



Joonwon Lee , Umakishore Ramachandran

ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture May 1990

Volume 18 Issue 3

Introducing private caches in bus-based shared memory multiprocessors leads to the cache consistency problem since there may be multiple copies of shared data. However, the ability to snoop on the bus coupled with the fast broadcast capability allows the design of special hardware support for synchronization. We present a new lock-based cache scheme which incorporates synchronization into the cache coherency mechanism. With this scheme high-level synchronization primitives as well as low-le ...

7 Compiler techniques for data partitioning of sequentially iterated parallel 77%



loops

David E. Hudak , Santosh G. Abraham

ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing June 1990

Volume 18 Issue 3

This paper uses bottom-up, static program partitioning to minimize the execution time of parallel programs by reducing interprocessor communication. Program partitioning is applied to a parallel programming construct known as a sequentially iterated parallel loop. This paper develops and evaluates compiler techniques to automatically generate data partitions for sequentially iterated parallel loops that minimize interprocessor communication. These techniques could be included as a communica ...

8 Disk-directed I/O for MIMD multiprocessors 77%



David Kotz

ACM Transactions on Computer Systems (TOCS) February 1997

Volume 15 Issue 1

Many scientific applications that run on today's multiprocessors, such as weather forecasting and seismic analysis, are bottlenecked by their file-I/O needs. Even if the multiprocessor is configured with sufficient I/O hardware, the file system software often fails to provide the available bandwidth to the application. Although libraries and enhanced file system interfaces can make a significant improvement, we believe that fundamental changes are needed in the file server software. We prop ...

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1 Architectural impact of secure socket layer on Internet servers
Kant, K.; Iyer, R.; Mohapatra, P.;

Computer Design, 2000. Proceedings. 2000 International Conference on , 17-21 2000

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2 Bus buffer modeling and optimization in video processing IP
Kun-Bin Lee; Chia-Hsing Lin; Chein-Wei Jen;

Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on , Volume: 3 , 5-8 Sept. 1999

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3 A bandwidth-efficient implementation of mesh with multiple broadcast
Jong Hyuk Choi; Bong Wan Kim; Kyu Ho Park; Kwang-Il Park;

Parallel Processing, 1999. Proceedings. 1999 International Conference on , 21-24 Sept. 1999

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4 An approach to verify a large scale system-on-a-chip using symbolic checking
Takayama, K.; Satoh, T.; Nakata, T.; Hirose, F.;

Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceed International Conference on , 5-7 Oct. 1998
Page(s): 308 -313

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5 Design and performance evaluation of an adaptive cache coherence protocol

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... of creating Verilog or VHDL simulation **test cases**. These **test cases** are typically ... specifies the seed to be used to generate random **bus transactions** for the PLB ...
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... It provides hardware for counting certain events associated with PLB **bus transactions**. ... BFC is a Perl program that parses the **test cases** written in the BFL and ...
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